

CLAIMS:

1. A FIFO memory device comprising a storage stage and input stage, the storage stage comprising a plurality of non-volatile storage elements and the input stage comprising a plurality of volatile storage elements.
 - 5 2. A FIFO memory device according to claim 1, wherein the storage stage comprises a non-volatile FIFO memory device.
 3. A FIFO memory device according to claim 1 or 2, wherein the input stage comprises a volatile FIFO memory device.
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4. A FIFO memory device according to any one of the preceding claims, wherein the memory device further comprises means for monitoring the status of the input stage and/or storage stage.
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5. A FIFO memory device according to claim 4 wherein the monitoring means includes a counter indicating the number of empty spaces.
 6. A FIFO memory device according to any one of the preceding claims wherein the input stage and storage stage are connected in series.
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7. An integrated circuit comprising at least one memory device according to any one of the preceding claims.